CLAIMS

What is claimed is:

1. A system comprising:

a first transmitter having a first data input terminal that receives first transmit data, a first transmit clock terminal that receives a first transmit clock of a transmit frequency, and a first data output terminal that transmits the first transmit data synchronized with the first transmit clock;

a second transmitter having a second data input terminal that receives second transmit data, a second transmit clock terminal that receives a second transmit clock of the transmit frequency, and a second data output terminal that transmits the second transmit data synchronized with the second transmit clock; and

a phase adjustment circuit that derives the first transmit clock from a reference clock signal and adjusts the first transmit clock to vary the phase of the first transmit data with respect to the second transmit data.

2. The system of claim 1, wherein the phase adjustment circuit dynamically varies the phase of the first transmit data with respect to the second transmit data.

3. The system of claim 2, wherein the phase-adjustment circuit includes a phase mixer.

4. The system of claim 3, wherein the phase-adjustment circuit further includes a phase control circuit coupled to the phase mixer.

5. The system of claim 2, wherein the phase-adjustment circuit includes a counter that issues

periodic select signals to the phase mixer during transmission of at least one of the first and second transmit data.

6. The system of claim 2, wherein the phase-adjustment circuit includes a phase mixer, the system further comprising a locked-loop circuit connected to the mixer, and wherein the locked-loop circuit delivers a plurality of reference-clock phase vectors to the phase mixer.

7. The system of claim 1, further comprising:

a first transmission channel coupled to the first transmitter output terminal, wherein the first transmission channel conveys the first transmitted data;

a second transmission channel coupled to the second transmitter output terminal, wherein the second transmission channel conveys the second transmitted data; and

a receiver having a receiver input node coupled to the first transmitter output terminal via the first transmission channel, wherein the receiver input node receives the first transmitted data, and wherein the receiver input node receives an artifact of the second transmitted data as crosstalk coupled from the second transmission channel to the first transmission channel.

8. A system comprising:

a transmitter having a data input terminal that receives first transmit data, a transmit clock terminal that receives a transmit clock of a transmit frequency, and a data output terminal that transmits the first transmit data synchronized with the transmit clock;

a first communication channel coupled to the first data output terminal, wherein the first communication channel receives the first transmit data;

a first receiver having a first receiver input node coupled to the first data output terminal via the first communication channel, wherein the first receiver input node receives the first transmitted data from the transmitter;

a second communication channel that conveys second transmit data;

a second receiver having a second receiver input node coupled to the second communication channel, wherein the second receiver input nodes receives the second transmit data and crosstalk artifacts of the first transmitted data; and

a phase adjustment circuit connected to the transmit clock terminal of the transmitter, wherein the phase adjustment circuit adjusts the first transmit clock to vary the timing of the crosstalk artifacts with respect to the second transmit data.

9. The system of claim 8, wherein the second communication channel conveys the second transmit data at the transmit frequency.

10. The system of claim 8, wherein the phase adjustment circuit dynamically varies the timing of the first transmit data with respect to the second transmit data.

11. The system of claim 10, wherein the phase-adjustment circuit includes a phase mixer.

12. The system of claim 10, wherein the phase-adjustment circuit further includes a phase control circuit connected to the phase mixer.

13. The system of claim 12, wherein the phase-adjustment circuit includes a counter that issues periodic select signals to the phase mixer during transmission of at least one of the first and second transmit data.

14. The system of claim 10, wherein the phase-adjustment circuit includes a phase mixer, the system further comprising a loop circuit connected to the mixer, and wherein the loop circuit delivers to the phase mixer a plurality of reference-clock phase vectors.

15. The system of claim 8, wherein the loop circuit comprises a phase-locked loop.

16. A transceiver comprising:

a reference clock source that produces a reference clock;

a loop circuit coupled to the reference clock source, wherein the loop circuit derives a plurality of clocks of different clock phases from the reference clock;

a transmit mixer coupled to the loop circuit, wherein the transmit mixer derives a transmit clock from the clocks of different clock phases, the transmit mixer including a phase control port;

a transmit phase controller coupled to the phase control port, wherein the transmit phase controller issues transmit-phase control signals via the phase control port to alter the phase of the transmit clock; and

a transmitter that transmits data samples synchronized with the transmit clock.

17. The transceiver of claim 16, wherein the transmitter phase controller issues a plurality of the transmit-phase control signals as the transmitter transmits the data samples.

18. The transceiver of claim 16, further comprising:

a receive mixer coupled to the loop circuit, wherein the receive mixer derives a receive clock from the clocks of different phases;

a receive phase controller coupled to the second phase control port, wherein the receive phase controller issues receive-phase control signals via the second phase control port to alter the phase of the receive clock; and

a receiver that receives data samples synchronized with the receive clock.

19. The transceiver of claim 16, further comprising a resynchronizer that produces the transmit data synchronized with the transmit clock from transmit data synchronized with a second clock.

20. The transceiver of claim 19, further comprising a serializer disposed between the resynchronizer and the transmitter.

21. A method comprising:

transmitting first and second data signals timed to respective first and second transmit clocks to respective first and second receivers;

monitoring an output of the second receiver for errors induced by the first data signal; and

adjusting, in response to the monitoring, the timing of the first transmit clock in relation to the second transmit clock.

22. The method of claim 21, wherein the monitoring includes calculating the bit-error rate of the second receiver.

23. The method of claim 22, wherein the adjusting reduces the bit-error rate.

24. The method of claim 21, further comprising dynamically adjusting the timing of the first

transmit clock relative to the second transmit clock while transmitting the first and second data signals.

25. A method comprising:

transmitting first, second, and third data signals timed to respective first and second transmit clocks to respective first and second receivers over respective first and second communication channels, wherein the first data signal induces crosstalk artifacts in the second communication channel; and

adjusting the phase of the first transmit clock in relation to the second transmit clock while transmitting the first and second data signals.

26. A system comprising:

a first transmitter having a first data input terminal that receives first transmit data, a first transmit clock terminal that receives a first transmit clock of a transmit frequency, and a first data output terminal that transmits the first transmit data synchronized with the first transmit clock;

a second transmitter having a second data input terminal that receives second transmit data, a second transmit clock terminal that receives a second transmit clock of the transmit frequency, and a second data output terminal that transmits the second transmit data synchronized with the second transmit clock; and

phase-adjusting means for adjusting the first transmit clock to vary the timing of the first transmit data with respect to the second transmit data.

27. The system of claim 26, wherein the phase-adjusting means dynamically varies the timing

of the first transmit data with respect to the second transmit data.

28. The system of claim 27, wherein the phase-adjusting means issues periodic select signals to the phase mixer during transmission of at least one of the first and second transmit data.

29. A communication system comprising:

a. a first transmitter driven by a first transmit clock signal of a first phase, the first transmitter adapted to transmit first data synchronized to the first transmit clock signal;

b. a first communication channel coupled to the first transmitter and conveying the first transmit data;

c. at least one aggressor transmitter driven by a second transmit clock signal of an aggressor data phase, the aggressor transmitter adapted to transmit second data synchronized to the second transmit clock signal;

d. a second communication channel coupled to the second transmitter and conveying the second transmit data; and

e. a victim receiver coupled to the first communication channel and adapted to sample the first transmit data using a receive clock signal of a victim data phase, the victim receiver additionally receiving cross-talk artifacts of the second transmit data;

f. wherein at least one of the aggressor transmitter and the victim receiver includes phase-adjustment circuitry adapted to alter the aggressor data phase relative to the victim data phase to reduce crosstalk from the aggressor transmitter to the victim receiver.

30. The communication system of claim 29, wherein the crosstalk is FEXT.

31. The communication system of claim 30, wherein the crosstalk is NEXT.